

PRR20

ISO 9001:2015 AICTE-CIT GOLD Category Institute NAAC 'A' Grade Institute (CGPA: 3.21) NIRF-2020 Rank Band: 201-250

KAKATIYA INSTITUTE OF TECHNOLOGY & SCIENCE
 Opp : Yerragattu Gutta, Hasanparthy (Mandal), WARANGAL - 506 015, Telangana, INDIA.
 काकतीय प्रौद्योगिकी एवं विज्ञान संस्थान, वरंगल - ५०६ ०१५ तेलंगाना, भारत
 కాకతీయ సాంకేతిక విజ్ఞాన శాస్త్ర విద్యాలయం, వరంగల్ - 506 001 తెలంగాణ, ప్రభుత్వం
 (An Autonomous Institute under Kakatiya University, Warangal)
 (Approved by AICTE, New Delhi; Recognised by UGC under 2(f) & 12(B); Sponsored by KASABA EDUCATION SOCIETY)
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2023-24
2ES&VLSI
I-FLOOR
B I 220
w.e.f.
04.03.2024

ACADEMIC YEAR 2023-24 : EVEN SEMESTER

SECOND SEMESTER TIMETABLE

M.Tech. ES&VLSI

Class Teacher: Dr. K. Srinivas

DAY/TIME	9.10 - 10.00	10.00 - 10.50	10.50 - 11.40	11.40 - 12.30	L U N C H B R E A K	13.30 - 14.20	14.20 - 15.10	15.10 - 16.00
MONDAY	AICD	ESDWRTOS	LVLSI	ESDWRTOS (T)		AICD (T)	Mini Project	
TUESDAY	ESDWRTOS	→AICD Lab← BJ				DM SH-3-2	ASCD	ASCD (T)
WEDNESDAY	ASCD	LVLSI	AICD	Library		→ASCD Lab← CHP, VSR		
THURSDAY	LVLSI	→ASCD Lab← CHP, MQ				DM SH-3-2	Library	Library
FRIDAY	→AICD Lab← BSK			ESDWRTOS		AICD	ASCD	LVLSI (T)
SATURDAY								

Course Title	Course Code & Course Name		Course Faculty
AICD	P20EV201: Analog IC Design	-	Dr. B. Jeevan(BJ)
ASCD	P20EV202: Advanced System On Chip Design	-	Dr. V. Raju (VR)
LVLSI	P20EV203A: Low Power VLSI Design	-	Dr. K. Srinivas (KSC)
ESDWRTOS	P20EV204A: Embedded Systems Design with RTOS	-	Sri B. Shashikanth(BSK)
DM	P20AC208D: Disaster Management	-	Ms. M. Soujanya Laxmi
AICD Lab	P20EV205: Analog IC Design Laboratory	-	Sri B. Shashikanth (BSK), Dr. B. Jeevan(BJ)
ASCD Lab	P20EV206: Advanced System On Chip Design Laboratory	-	Sri Ch. Pawan Kumar (CHP) , Sri V. Shoban Reddy (VSR), Sri Md. Abdul Mugeem (MQ)
Mini Project	P20EV207: Mini Project with Seminar	-	Dr. B. Jeevan (BJ)

[Signature]
 Faculty I/c,
 Dept. Timetables

[Signature]
 Faculty I/c,
 Overall Timetables

[Signature]
 Head of the Department

[Signature]
 Dean, AA

[Signature]
 Principal