P14VE101  Digital Design

Class: M.Tech. I Semester  Branch: VLSI & Embedded Systems

Teaching Scheme:

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Examination Scheme:

- Continuous Internal Evaluation: 40 marks
- End Semester Exam: 60 marks

Course Learning Objectives:

- To introduce NMOS Logic Gates, Simple CMOS Logic Gates and their analysis.
- To introduce Sequential System Design Techniques.
- To introduce computer-aided minimization procedures such as the CAMP and IISE algorithms.
- To introduce PLDs and Advanced FPGA concepts suitable for VLSI circuits

UNIT - I (12+4)
The Basics: Simple NMOS Logic Gates, Simple CMOS Logic Gates, Transfer Curves and Noise margins, Gate Delays and Rise and Fall Times, Transient Response, an RC Approximation to the Transient Response of a CMOS Inverter.


UNIT - II (12+4)

UNIT - III (12+4)


UNIT - IV (12+4)
Design using PLAs, PALs, PLDs Programmable Logic Arrays: PLA minimization and PLA folding.
Text Books:
3  Samuel C.Lee and B.S.Sonde, “Digital Circuits And Logic Design”, PHI, New Delhi
4  Stephen M.Trimberger “Field Programmable Gate Array Technology” Springer International Edn.

Course Learning Outcomes:
After completion of the course the student will be able to
- Design CMOS Logic Gates with specified noise margin and propagation delay.
- Design Combinational Logic blocks.
- Learn Synchronous System Design Techniques
- Understand PLDs and Xilinx FPGA concepts
P14VE102 VLSI Technology

Class: M.Tech. I Semester Branch: VLSI & Embedded Systems

Teaching Scheme: Examinaton Scheme:

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Course Learning Objectives:
- To introduce system design methodology and tools
- To introduce the concepts of Scalable CMOS design rules
- To introduce the concepts of cell based layout design, interconnect delay modeling, floor planning, and routing.
- To introduce different steps involved in fabrication of chip

UNIT - I (12+4)

Basic concepts of Physical Design - layout of basic structures – wells, FET, BJT, resistors, capacitors, contacts, vias and wires (Interconnects). Parasitics – latch up and its prevention, cell concepts.

Design rules – fabrication errors – scalable design rules. Scalable CMOS (SCMOS) design rules, layout design, and stick diagrams, Hierarchical stick diagrams.

UNIT - II (12+4)

Cell concepts – cell based layout design – Wein berger image array – physical design of logic gates – NOT, NAND and NOR – design hierarchies. System level physical design, large scale physical design, interconnects delay modeling, floor planning, routing, clock distribution.

UNIT - III (12+4)

Crystal structure, Crystal growth and vapour phase epitaxy. Unit processes for VLSI-Oxidation, Photolithography, diffusion and ion implantation.

UNIT - IV (12+4)

Deposition of metal and dielectric films by vacuum evaporation, sputtering and CVD techniques, Wet chemical and Dry etching techniques.
Text Books:

Reference Books:

Course Learning Outcomes:
After completion of the course the student will be able to
- understand concepts of physical design.
- understand CMOS design rules.
- understand System level physical design.
- understand different steps involved in fabrication.
P14VE103  Discrete Mathematics & Optimization Techniques

Class: M.Tech. I Semester  Branch: VLSI & Embedded Systems

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Examination Scheme:

| Continuous Internal Evaluation: | 40 marks |
| End Semester Exam : | 60 marks |

Course Learning Objectives:
- To introduce the methods of optimization of both linear and non-linear objectives under a set of constraints.
- To introduce the techniques of solving decision making problems and analyze them in a competitive situations to get optimal output.
- To introduce the concepts and determination of optimal flow in a transport network and analysis of network scheduling by CPM-PERT with their practical applications.
- To introduce the basic concepts of Fuzzy sets, Fuzzy operations, Fuzzy logic and their Engineering applications

UNIT - I (12+4)
Constrained optimization: Linear programming concepts: Simplex method, Artificial variables method, Duality and Dual simplex method. Integer linear programming: Branch and Bound algorithm, Cutting plane algorithm.


UNIT - II (12+4)

UNIT - III (12+4)

UNIT - IV (12+4)
Text Books:

Reference Books:

Course Learning Outcomes:
After completion of the course the student will be able to
- Solve any type of LPP and discuss the nature of the solution.
- Solve a class of non-linear programming problems with different types of constraints.
- Identify the importance of decision making systems and find an optimal solution of the problem given different types of nature of states.
- Analyze different strategies of a Game between two objects under conflicting situations.
- Develop an algorithm for solving problems of Game theory.
- Find a maximal flow of commodities in a transport network using different methods.
- Discuss different network based methods designed to assist in the planning, scheduling and control of projects.
- Identify the differences between Crisp sets and Fuzzy sets and the related properties.
- Differentiate between Classical systems and Fuzzy systems in order to solve the problems based on Fuzzy logic.
P14VE104 Embedded System Design

Class: M.Tech. I Semester  Branch: VLSI & Embedded Systems

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Examination Scheme:

- Continuous Internal Evaluation: 40 marks
- End Semester Exam: 60 marks

Course Learning Objectives:

- To introduce various hardware and software embedded structures in real time applications
- To introduce the basic design concepts of embedded systems
- To introduce the Communication protocol concepts of embedded systems
- To introduce methods Inter processor communication

UNIT – I (12+4)
Introduction to Embedded Systems:
Processor and Memory Selection:
Different Types of Processor Technologies, Processor Selection for an Embedded System, Different Types of Memory Devices, Memory Selection for an Embedded System.

UNIT – II (12+4)
Device Drivers and Interrupts Servicing Mechanism:
Different types of Interrupts, Interrupt Servicing Mechanism, Device Servicing using ISR, Device Drivers, Parallel Port and Serial Port Device Drivers and Device driver Programming

UNIT – III (12+4)
Software Engineering Practices in the Embedded Software Development Process:

UNIT – IV (12+4)
Programming models for Single and Multiprocessor Systems: DFG, CDFG, FSM, Petri nets, SDFG, HSDF, APEG and MTG
Inter-Process Communication and Synchronization of Processes, Tasks And Threads: Multiple Processes in an Application, Problem of Sharing Data by Multiple Tasks and Routines, Inter Process Communication
Text Books:

Reference Books:

Course Learning Outcomes:
After completion of the course the student will be able to
- Design a embedded system for real time applications
- Handle interrupts in embedded system development
- Understand inter processor communication and synchronization
P14VE105 A Hardware Description Languages

Class: M.Tech. I Semester
Branch: VLSI & Embedded Systems

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Examination Scheme:

| Continuous Internal Evaluation: | 40 marks |
| End Semester Exam : | 60 marks |

Course Learning Objectives:
- To introduce Dataflow & structural modeling programs using VHDL.
- To introduce Sequential modeling using VHDL.
- To introduce design styles used in HDLs.
- To introduce the design using Verilog HDL

UNIT - I (12+4)

UNIT - II (12+4)
Concurrent Code: Concurrent versus Sequential, Using Operators, WHEN, Generate and Block, Sequential Code: Process, Signals and Variables, IF, WAIT, CASE, Using Sequential, Code To Design Combinational Circuits

UNIT - III (12+4)
State Machines: Introduction, Design Style #1, Design Style #2 (Stored Output), Encoding Style: From Binary to One-Hot

UNIT - IV (12+4)

Text Books:
3. Samir palnitkar, ”Verilog HDL”,Pearson Education Asia ,New Delhi,2001

Course Learning Outcomes:
After completion of the course the student will be able to
- Write Dataflow & structural modeling programs using VHDL.
- Differentiate Concurrent & Sequential Design.
- Design State Machines with different styles.
- Learn Concepts of Verilog HDL.
P14VE105 B  Semiconductor Device Modeling

Class: M.Tech. I Semester  Branch: VLSI & Embedded Systems

Teaching Scheme:  Examination Scheme:

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Continuous Internal Evaluation: 40 marks  End Semester Exam : 60 marks

Course Learning Objectives:
- To introduce the concepts of energy band in solids and design of bipolar devices.
- To introduce performance characteristics of CMOS devices.
- To introduce different MOSFET DC Models.
- To introduce Optoelectronic Devices and Spice Models for Semiconductor devices

UNIT – I (12+4)

UNIT – II (12+4)
CMOS Performance characteristics: Basic CMOS Circuit Elements, Parasitic Elements, Sensitivity of CMOS delay to device parameters, Performance characteristics of Advanced CMOS Devices.

UNIT – III (12+4)

UNIT – IV (12+4)
Optoelectronics Devices: Light emitting diodes, Lasers, Photoconductors, Junction Photodiodes, Avalanche Photodiodes, Solar Cells, SPICE Models for Semiconductor Devices: MOSFET Level 1, Level 2 and level 3 model, Model parameters; SPICE models of p-n diode and BJT.
Text Books:

Reference Books:

Course Learning Outcomes:
After completion of the course students will be able to
- understand bipolar device models and apply SPICE models to Semiconductor Devices.
- understand CMOS Performance characteristics.
- analyze MOSFET DC models
- describe the basic operation of Optoelectronics Devices.
P14VE105C Scripting Languages for VLSI Design Automation

Class: M.Tech. I Semester  Branch: VLSI & Embedded Systems

Teaching Scheme:  Examination Scheme:

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Continuous Internal Evaluation: 40 marks
End Semester Exam: 60 marks

Course Learning Objectives:
- To introduce the basics of various scripting languages such as PERL, CGI, VB Script, Java Script.
- To introduce the programs based on PERL.
- To introduce the concepts of inter processes communication threads.
- To introduce programming concepts in PERL, VB Script and JAVA script.

UNIT - I (12+4)
Overview of Scripting Languages- PERL, CGI, VB Script, Java Script.

UNIT - II (12+4)
PERL:
Operators, Statements Pattern Matching etc. Data Structures, Modules, Objects, Tied Variables

UNIT - III (12+4)
Inter process Communication Threads, Compilation & Line Interfacing.

UNIT - IV (12+4)
Debugger Internal & Externals Portable Functions. Extensive Exercises for Programming in PERL.
Other Languages:
Broad Details of CGI, VB Script, Java Script with Programming Examples.

Text Books:
2. Larry Wall, Tom Christiansen, John Orwant, “Programming PERL”.

Course Learning Outcomes:
After completion of the course students will be able to
- Learn the basics of various scripting languages.
- Understand the programs based on PERL.
- Get familiarized with the inter process communication threads.
- Learn programming skills in PERL, VB Script and JAVA script.
P14VE105D  Computer Aided Circuit Simulation

Class: M.Tech. I Semester  Branch: VLSI & Embedded Systems

Teaching Scheme:                  Examination Scheme:

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Continuous Internal Evaluation: 40 marks
End Semester Exam: 60 marks

Course Learning Objectives:
- To formulate equations and solve nonlinear networks
- To introduce special classes of multistep methods for the solution of electrical networks.
- To introduce general purpose circuit simulators.
- To introduce physical or empirical models of semiconductor parameters in small signal analysis

UNIT – I (12+4)
Formulation of network equations: Nodal, mesh, modified nodal and hybrid analysis equations.; Sparse matrix techniques; Solution of nonlinear networks through Newton-Raphson technique.; Multistep methods: convergence and stability;

UNIT – II (12+4)
Special classes of multistep methods: Adams-bashforth, Adams-Moulton and Gear's methods; Solution of stiff systems of equations; Adaptation of multistep methods to the solution of electrical networks;

UNIT – III (12+4)
General purpose circuit simulators.; Review of semiconductor equations (Poisson, continuity, drift-diffusion, trap rate). Finite difference formulation of these equations in 1D and 2D. Grid generation.;

UNIT – IV (12+4)
Physical/empirical models of semiconductor parameters (mobility, lifetime, band gap, etc.); Computation of characteristics of simple devices (p-n junction, MOS capacitor, MOSFET, etc.); Small-signal analysis.

Text Books:

Course Learning Outcomes:
After completion of the course students will be able to
- Solve nonlinear networks
- apply multistep methods and solve electrical networks.
- Apply general purpose circuit simulators.
- Use physical and empirical models in computation of semiconductor device characteristics.
P14VE106A  Advanced Microprocessor and Microcontroller

Class: M.Tech. I Semester                      Branch: VLSI & Embedded Systems

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Examination Scheme:

- Continuous Internal Evaluation: 40 marks
- End Semester Exam: 60 marks

Course Learning Objectives:

- To expose the students to the fundamentals of microprocessor architecture.
- To introduce the advanced features in microprocessors and microcontrollers.
- To enable the students to understand various microcontroller architectures

UNIT - I (12+4)
16 Bit Microcontrollers: 8096/196 family microcontrollers Architecture, instruction set programming, interrupts, timers, serial communication programming

UNIT - II (12+4)
MC68HC11 family microcontrollers: Architecture, interrupts, timers.

Instruction set addressing modes - operating modes programming - Interrupt system - RTC-Serical Communication Interface - A/D Converter PWM and UART.

UNIT - III (12+4)
Interfacing Methods: Switch, key board, display (LED, LCD), printer, motor, memory ADC, DAC I/o interfacing methods, C programming basics for Microcontrollers

UNIT - IV (12+4)
Text Books:

Course Learning Outcomes:
After completion of the course the student will be able to:

- The student will be able to work with suitable microprocessor / microcontroller for a specific real world application
P14VE106B  Data Communication Computer Networks

Class: M.Tech. I Semester  Branch: VLSI & Embedded Systems

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Examination Scheme:

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Course Learning Objectives:

- To introduce transmission media protocols & routing
- To introduce Access techniques, IEEE 802 standards, switched and Fast Ethernet.
- To introduce Network Protocols & Inter-networking
- To introduce the concepts of Quality of service, network security and management.

UNIT – I (12+4)
Introduction to Network components, switching technologies, topologies, transmission media, protocols & routing.
WAN, NAN, LAN. Queuing theory models and applications computer networks, Data communication concepts – asynchronous & synchronous transmission, error correction codes & detectors.

UNIT – II (12+4)
Transmission Protocols:
STOP – START, BSC, SDLC, HDLC, Retransmission techniques. LAN – components, Topologies, Access techniques, IEEE 802 standards, switched and Fast Ethernet, FDDI & SONET.

UNIT – III (12+4)

UNIT - IV (12+4)
Text Books:

Reference Books:

Course Learning Outcomes:
After completion of the course students will be able to
- understand protocols & routing, switching technologies, topologies, transmission media and its applications.
- understand IEEE 802 standards, Fast Ethernet, FDDI & SONET.
- understand OSI model – X.25, TCP/IP layers in an Internet.
- understand Quality of service and ideas on network security and management
P14VE106C  Data Structures & Algorithm Analysis

Class: M.Tech. I Semester  
Branch: VLSI & Embedded Systems

Teaching Scheme: 

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Examination Scheme: 

- Continuous Internal Evaluation: 40 marks
- End Semester Exam: 60 marks

Course Learning Objectives:
- To introduce concepts of linked lists, stacks and queues
- To introduce sorting techniques.
- To introduce searching techniques and its applications.
- To introduce the techniques for designing algorithms

UNIT - I (12+4)
Introduction to DS:
Lists, Stacks and queues, abstract data types , the list ADT-the stack ADT, the queue ADT
Trees: Preliminaries, binary trees , the search tree ADT, binary search trees , AVL trees, splay trees, B- Trees.

UNIT - II (12+4)
Sorting
Internal sorting, preliminaries, insertion sort, a lower bound for simple sorting Algorithms, Shell sort, heap sort, merge sort, quick sort, bucket sort,, external sorting.

UNIT – III (12+4)
Graph algorithms:
Hashing: Hash function, separate chaining, open addressing, rehashing, extendable hashing.

UNIT – IV (12+4)
Algorithm design techniques:
Greedy algorithms, divide and conquer, dynamic programming
Introduction to NP-completeness:
Easy versus hard, the class NP,NP-complete problems.
Text Books:

Reference Books:

Course Learning Outcomes:
After completion of the course students will be able to
- write programs for linked lists, stacks and queues
- analyze and compare sorting techniques
- Apply searching techniques in data analysis
- understand the algorithm development methods
P14VE106D  Digital Filter Design

Class: M.Tech. I Semester  Branch: VLSI & Embedded Systems

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### Examination Scheme:

- Continuous Internal Evaluation: 40 marks
- End Semester Exam: 60 marks

### Course Learning Objectives:

- To introduce the concepts of the basic Multirate techniques like interpolation, decimation of DSP.
- To learn stationary random process, Rational power spectra Auto-correlation sequence.
- To introduce the Optimum reflection coefficients for the Lattice forward and backward Predictors.
- To introduce the Properties of Linear Prediction error filters, orthogonality principle in Linear Mean-Square Estimation

### UNIT – I (12+4)

Multirate Digital Signal Processing:

### UNIT – II (12+4)

Linear Prediction and Optimum Linear Filters:
Representation of a stationary random process. Rational power spectra-AR, MA & ARMA processes. Relationship between the filter parameters and Auto-correlation sequence. Forward and Backward linear prediction

### UNIT – III (12+4)

Optimum reflection coefficients for the Lattice forward and backward predictors. AR process and linear prediction. Solution of Normal equations. Levinson-Durbin algorithm. The Schur algorithm. Pipelined architecture for implementing the Schur algorithm

### UNIT - IV (12+4)


### Text Books:

Reference Books:

Course Learning Outcomes:
After completion of the course students will be able to
- understand the practical sampling-rate converters interpolators and decimators.
- Identify the processes characteristics from the transfer function
- Use different algorithms such as Levinson-Durbin algorithm, Schur algorithm
- learn various Properties of Linear Prediction error filters
P14VE107  VLSI Technology Laboratory

Class: M.Tech. I Semester  Branch: VLSI & Embedded Systems

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Examination Scheme:

| Continuous Internal Evaluation: | 40 marks |
| End Semester Exam : | 60 marks |

Course Learning Objectives:

- To introduce Layouts of basic devices and algorithms
- To introduce placing and routing algorithms
- To introduce concepts of interconnect delay modelling
- To introduce automatic layout tools and design rule checkers

List of Experiments:

1. Layout of Basic Devices
2. Partitioning Algorithms
3. Place and Route Algorithms
4. Floor Planning and Pin Assignment
5. Routing, DRC & Automatic Layout Tools
6. Clock distribution
7. Interconnect Delay modeling
9. Mini Project – 2

Note: As a part of this Laboratory course students has to takeup TWO mini projects.

Report is to be submitted

Course Learning Outcomes:

After completion of the course students will be able to

- To learn Layouts of basic devices and algorithms
- To understand placing and routing algorithms
- To learn concepts of interconnect delay modelling
- To understand concepts of automatic layout tools and design rule checkers
P14VE108  Digital Design Laboratory

Class: M.Tech. I Semester  Branch: VLSI & Embedded Systems

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Examination Scheme:

| Continuous Internal Evaluation: | 40 marks |
| End Semester Exam: | 60 marks |

Course Learning Objectives:

- To introduce modeling styles used in Verilog
- To introduce Sequential System Design using Verilog.
- To introduce implementation of circuits using Bit-wise, logical and reduction operators.
- To introduce implementation of Finite State Machines and Sequence Detectors

List of Experiments: (Using Verilog)

Simulation of

1. Ripple Carry Adder using Gate Level modeling.
3. Ripple Counter in Data Flow modeling.
6. 8 function ALU that takes 4-bit inputs in behavioral modeling.
7. Finite State Machines realization.
8. Sequence Detectors.
9. Mini-projects-2

Note: As a part of this Laboratory course students has to takeup TWO mini projects.

Report is to be submitted

Course Learning Outcomes:

After completion of the course students will be able to
- design Logic Gates using HDLs.
- design Combinational Logic blocks.
- design Synchronous System Design using HDLs.
- design state machines.
P14VE109  Seminar

Class: M.Tech. I Semester  Branch: VLSI & Embedded Systems

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Examination Scheme:  

| Continuous Internal Evaluation: | 100 marks |
| End Semester Exam: | ---- |

1. There shall be only Continuous Internal Evaluation (CIE) for Seminar, which includes Report Submission & Presentation.

2. A teacher will be allotted to a student for guiding in 
   (i) selection of topic 
   (ii) report writing 
   (iii) Presentation (PPT) before the DPGRC on a pre notified date.
P14VE201  Mixed Signal Design

Class: M.Tech. II Semester  Branch: VLSI & Embedded Systems

Teaching Scheme:  Examination Scheme:

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Continuous Internal Evaluation:  40 marks
End Semester Exam :  60 marks

Course Learning Objectives:
- To introduce the concepts of Analog design techniques.
- To introduce the design techniques for differential amplifiers and operational amplifiers.
- To introduce concepts of MOS OPAMPS with cascade.
- To introduce concepts of data converters.

UNIT – I (12+4)

UNIT – II (12+4)
Differential amplifiers – single ended and Differential operation, Basic Differential pair, common mode response and Differential pairs with MOS loads. Operational amplifiers – General considerations, one stage OPAMPS, two stage OPAMPS. Gain Boosting, comparison, common mode feedback, Input range limitations, slew rate and power supply rejections.

UNIT – III (12+4)
Two stage MOS OP-AMP with cascodes. MOS Telescopic cascode OPAMP. MOS Folded cascode OP-AMP. Current feedback OPAMPS. Stability and frequency compensation of OP-AMPS, Gain margin and Phase margin OPAMPS.

UNIT – IV (12+4)
Data converter fundamentals: Ideal D/A converter, Ideal A/D converters, Quantization noise, signed codes, performance limitations.

D/A Converters: - decoder based converter, binary – Scaled Converters, Thermometer code converter, hybrid converters.

Text Books:
1. R. Gregorian, Temes, “Analog MOS integrated circuits for Signal processing”.
2. R. Gregorian, “Introduction to CMOS opamps and comparators”.
5. B. Razavi, “Monolithic Phase-locked loops and clock recovery circuits”.

Course Learning Outcomes:
After completion of the course students will be able to
- understand the significance of analog design and its applications
- design and analyze differential amplifiers and operational amplifiers
- acquire the ability design cascade amplifiers.
- understand the fundamentals of data converters.
P14VE202  RTOS for Embedded Systems

Class: M.Tech. I Semester  
Branch: VLSI & Embedded Systems

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Examination Scheme:

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<tr>
<th>Continuous Internal Evaluation:</th>
<th>40 marks</th>
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<td>End Semester Exam :</td>
<td>60 marks</td>
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Course Learning Objectives:

- To introduce the Unix Operating systems and process management
- To introduce the POSIX OS and IEEE standard 1003.13.
- To introduce the Real time Operating System concepts and kernel structure.
- To introduce the LINUX: Kernel real time extensions, scheduling threads, root file system and VX works OS.

UNIT – I (12+4)

Brief review of Unix operating systems (Unix kernel-file system, concept of process, concurrent execution and interrupt. process management-fork and execution. Programming with system calls, process scheduling .shell programming and filters).

Portable operating system interface (POSIX)-IEEE standard 1003.13 & POSIX real time profile .POSIX versus traditional unix signals overheads and timing predictability.

UNIT – II (12+4)

RTOS:
Real time systems concepts, open system architecture and issue .hard and soft real time system. RTOS kernel and issue in multi tasking-task assignment scheduling, inter task communication and synchronization. classical uniprocessor algorithms, scheduling, processor utilization. Application programming interface( API), RTAPI-capabilities

UNIT – III (12+4)

Commercial Real Time Operating Systems :
Micro C /OS-Real time Kernel &KERNEL structured and its working .application to embedded systems.(LYNOX)-Micro Kernel & Kernel plug-ins (KPIs ) for i/o support self hosted systems for embedded application).

PSOS systems-PSOS+(a Real time Kernel for a single micro processor application ) system Architecture and Modularity, feature: task management and scheduling, time management is i/o systems , driver interface environment -integrated development tools and host based debugging tools, brief ideas on PSOS+(a Microprocessor kernel & features).POSIX compliance, networking programming.

UNIT – IV (12+4)

LINUX: Kernel real time extensions, scheduling threads, root file system.
VX Works—POSIX Real Time Extensions, timeout features and wind semaphores and memory management - virtual to physical address mapping. Debugging tools and cross development environment. Comparison of commercial RTOS - LYNXOS, PSOS, QNX/Neutrino VLTS, VX Works, RTOS for embedded Applications.
Text Books:

Reference Books:

Course Learning Outcomes:
After completion of the course students will be able to
- understand the basic differences between different Operating systems.
- learn the POSIX OS and IEEE standard 1003.13.
- understand the Real time Operating System concepts and kernel structure.
- understand the concept of LINUX OS, VX works OS and other RTOS for embedded systems.
P14VE203  Low Power VLSI Design

Class: M.Tech. II Semester  Branch: VLSI & Embedded Systems

Teaching Scheme:

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Examination Scheme:

- Continuous Internal Evaluation: 40 marks
- End Semester Exam: 60 marks

Course Learning Objectives:
- To introduce Physics of power dissipation in CMOS
- To introduce low voltage CMOS circuit design styles.
- To introduce concepts of Low power architectures.
- To introduce Software design for low power

UNIT – I (12+4)

UNIT – II (12+4)
Design styles and testing – low voltage CMOS circuit design styles, leakage current in deep sub micron ICs, design issues, minimization of short channel effects (SCE) and hot carrier effects. Testing of deep sub micron ICs with elevated intrinsic leakage.

UNIT – III (12+4)
Low power architectures – MOS static RAM cells, banked organization SRAMS, reducing voltage swing on bit lines, write lines, driver circuits and sense amplifier circuits. Energy computing and recovery techniques – energy dissipation using an RC model, energy recovery circuit design, design with partially reversible logic and supply clock generation.

UNIT – IV (12+4)
Software design for low power - dedicated hardware Vs software implementation, power dissipation, estimation and optimization. Automated power code generation and co design for low power.

Text Books:

Course Learning Outcomes:
After completion of the course students will be able to
- know sources of power dissipation and design strategies for low power.
- analyze Design styles and testing.
- design MOS static RAM cells, banked organization SRAMS.
- know hardware & software co design for low power.
P14VE204 Hardware & Software Co-Design

Class: M.Tech. II Semester
Branch: VLSI & Embedded Systems

Teaching Scheme:
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Examination Scheme:
- Continuous Internal Evaluation: 40 marks
- End Semester Exam: 60 marks

Course Learning Objectives:
- To introduce the basic concepts of hardware software co-design.
- To introduce the Software and hardware Implementation of Data Flow.
- To understand the Analysis of Control Flow and Data Flow.
- To learn the concepts of System On Chip

UNIT – I (12+4)

UNIT – II (12+4)

UNIT – III (12+4)
Analysis of Control Flow and Data Flow: Data and Control Edges of a C Program, Implementing Data and Control Edges, Construction of the Control Flow Graph, Modern Bipolar, Transistor Structures, Construction of the Data Flow Graph, Finite State Machine with Datapath: Cycle-Based Bit-Parallel Hardware, Hardware Modules, Finite State Machines with Datapath, FSMD Design Example: A Median Processor

UNIT – IV (12+4)
Text Books:

Course Learning Outcomes:
After completion of the course students will be able to
- understand the Nature of Hardware and Software co design
- implement the Software and hardware for Data Flow.
- understand the Analysis of Control Flow and Data Flow, Finite State Machine With Datapath.
- design the System On Chip Architecture and various Processors
P14VE205A  ASIC Design

Class: M.Tech. I Semester  Branch: VLSI & Embedded Systems

Teaching Scheme:  Examination Scheme:

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Continuous Internal Evaluation: 40 marks
End Semester Exam: 60 marks

Course Learning Objectives:
- To introduce ASIC’s Design Flow & ASIC Library Design
- To introduce architectures of Actel & Xilinx ASICs.
- To introduce concepts of Programmable ASIC Design Software
- To introduce algorithms for ASICs/ SoCs as case studies

UNIT – I (12+4)

UNIT – II (12+4)
Programmable ASIC Logic Cells, Actel, Xilinx LCA., XC3000 CLB, XC4000 Logic Block, XC5200 Logic Block, Xilinx CLB Analysis,. Logic Expanders. Programmable ASIC I/O Cells, Totem-Pole Output, Mixed-Voltage Systems, Metastability, Xilinx I/O Block. Boundary Scan.

UNIT – III (12+4)
Programmable ASIC Interconnect and Programmable ASIC Design Software. Actel ACT, RC Delay in Antifuse Connections, Xilinx EPLD Logic Synthesis, FPGA Synthesis, Third-party Software. low level design entry, logic synthesis, simulation,

UNIT – IV (12+4)
High performance algorithms for ASICs/ SoCs as case studies – Canonic Signed Digit Arithmetic, KCM, Distributed Arithmetic, High performance filters using delta-sigma modulators, USB controllers, OMAP.
Text Books:

Reference Books:

Course Learning Outcomes:
After completion of the course students will be able to
- know Architecture of Programmable ASICs.
- analyze Programmable ASIC Logic Cells.
- understand Programmable ASIC Interconnect.
- write algorithms for ASICS/SoCs as case studies
P14VE205B  VLSI Signal Processing

Class: M.Tech. I Semester  Branch: VLSI & Embedded Systems

Teaching Scheme:

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Examination Scheme:

- Continuous Internal Evaluation: 40 marks
- End Semester Exam: 60 marks

Course Learning Objectives:
- To introduce techniques for altering the existing DSP structures to suit VLSI implementations.
- To introduce efficient design of DSP architectures suitable for VLSI

UNIT - I (12+4)
Introduction To Dsp Systems, Pipelining And Parallel Processing Of Fir Filters
Introduction to DSP systems – Typical DSP algorithms, Data flow and Dependence graphs – critical path, Loop bound, iteration bound, Longest path matrix algorithm, Pipelining and Parallel processing of FIR filters, Pipelining and Parallel processing for low power.

UNIT – II (12+4)
Retiming, Algorithmic Strength Reduction

UNIT – III (12+4)
Fast Convolution, Pipelining And Parallel Processing of Iir Filters

UNIT – IV (12+4)
Bit-Level Arithmetic Architectures
Bit-level arithmetic architectures – parallel multipliers with sign extension, parallel carry-ripple and carry-save multipliers, Design of Lyon’s bit-serial multipliers using Horner’s rule, bit-serial FIR filter, CSD representation, CSD multiplication using Horner’s rule for precision improvement, Distributed Arithmetic fundamentals and FIR filters.
### Text Books:


### Course Learning Outcomes:

After completion of the course the student will be able to

- Ability to modify the existing or new DSP architectures suitable for VLSI
P14VE205 C Microchip Fabrication Techniques

Class: M.Tech. II Semester

Teaching Scheme:

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Examination Scheme:

Continuous Internal Evaluation: 40 marks
End Semester Exam: 60 marks

Course Learning Objectives:

- To introduce International Technology Roadmap for Semiconductors
- To introduce Semiconductor Materials and Process Chemicals
- To introduce fabrication of wafers
- To introduce contamination control process yield

UNIT – I (12+4)
Semiconductor Industry - Birth of Industry, Evolution

UNIT – II (12+4)
Semiconductor Materials and Process Chemicals, Semiconductor Material Preparation, Crystal grown.

UNIT – III (12+4)

UNIT – IV (12+4)
Contamination Control:- Contaminants, Contamination, caused problems, Contaminant Sources, Clean Air Strategies, Clean Room Work Station Strategy and Clean Room Construction.

Text Books:
1. “Microchip Fab Techniques” by Peter Vanzant(4M Edition)

Course Learning Outcomes:

After completion of the course students will be able to

- understand International Technology Roadmap for Semiconductors
- understand Semiconductor Materials and how Process Chemicals.
- understand fabrication process of wafers.
- understand control process yield
P14VE205D  Design for Testability

Class: M.Tech. II Semester  Branch: VLSI & Embedded Systems

Teaching Scheme:

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Examination Scheme:

| Continuous Internal Evaluation: | 40 marks |
| End Semester Exam: | 60 marks |

Course Learning Objectives:
- To introduce the basic concepts of Design for Testability and modeling techniques
- To familiarize the testing for single stuck at faults, ATG pattern generation.
- To introduce the various DFT approaches for digital design.
- To learn the concepts of Built in Self test (BIST) and Memory BIST.

UNIT - I (12+4)
Introduction to Test and Design for Testability (DFT) Fundamentals

Modeling:

UNIT – II (12+4)
Testing for single stuck at faults (SSF) – Automated test pattern generation (ATPG/ATG) for SSFs in combinational and sequential circuits, Functional testing with specific fault models. Vector simulation – ATPG vectors, formats, Compaction and compression, Selecting ATPG Tool.

UNIT – III (12+4)
Design for testability – testability trade-offs, techniques. Scan architectures and testing – controllability and absorbability, generic boundary scan, full integrated scan, storage cells for scan design. Board level and system level DFT approaches. Boundary scan standards. Compression techniques – different techniques, syndrome test and signature analysis.

UNIT – IV (12+4)
Built-in self-test (BIST) – BIST Concepts and test pattern generation. Specific BIST Architectures – CSBL, BEST, RTS, LOCST, STUMPS, CBIST, CEBS, RTD, SST, CATS, CSTP, BILBO. Brief ideas on some advanced BIST concepts and design for self-test at board level.

Memory BIST (MBIST):
Memory test architectures and techniques – Introduction to memory test, Types of memories and integration, Embedded memory testing model. Memory test requirements for MBIST. Brief ideas on embedded core testing.
Text Books:

Course Learning Outcomes:
After completion of the course students will be able to
- understand the need of Testing and Testability
- learn different fault models and various test pattern generation methods.
- design the various DFT approaches for digital design and compression
- learn the different approaches for Built in Self test (BIST) and Memory BIST
P14VE206A  Industrial Applications of Embedded Microcontrollers

Class: M.Tech. II Semester  Branch: VLSI & Embedded Systems

Teaching Scheme:

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Examination Scheme:

| Continuous Internal Evaluation: 40 marks |
| End Semester Exam : 60 marks |

Course Learning Objectives:

- To introduce various process industrial applications
- To expose different interfacing technologies
- To Learn automobile industry applications
- To introduce wireless communication applications

UNIT – I (12+4)
Process Industrial applications robot ARM programming tools Optical rotary shaft, encoder, LVDT interfacing, special temperature load cell, ILC interface, software protocol, communication home automation & control/ applications

UNIT – II (12+4)
Zigbee interface, Ethernet interface, LED interface, LCD interface  GLID interface

UNIT – III (12+4)
Automobile industry applications motor control interface, CAN interface

UNIT – IV (12+4)
Wireless communication applications wireless networking and implementation of 802.11 with microcontroller

Text Books:
2 Rajiv Kapadia ,”8051 Microcontroller & Embedded Systems “

Course Learning Outcomes:

After completion of the course the student will be able to
- Understand process industrial applications
- Understand various interface technologies
- Understand automobile industry applications
- Understand wireless communication applications
P14VE206B  Advanced Computer Systems Architecture

Class: M.Tech. II Semester  Branch: VLSI & Embedded Systems

Teaching Scheme:  Examination Scheme:

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Continuous Internal Evaluation: 40 marks
End Semester Exam: 60 marks

Course Learning Objectives:
- To learn Multi processor systems and their bus communication
- To learn Principles of pipelining and parallelism
- To learn cache coherence, message passing mechanisms in Multi processors systems
- To learn Multi threading environments

UNIT – I (12+4)
Introduction to Parallel Processing: Evolution of computer systems, Parallelism in Uniprocessor systems, Parallel Computer Structures. Architectural classification schemes, parallel processing applications.


Program and Network Properties: Conditionals of Parallelism, Program Partitioning and Scheduling, Program Flow Mechanisms, System Interconnect Architectures

UNIT – II (12+4)
Principles of Pipelining and Vector processing: Pipelining, An overlapped parallelism, Instruction and arithmetic pipelines, principles of designing pipelined processors, vector processing requirements.

Pipeline computers and vectorization method: The space of pipelined computers, early vector processors, scientific attached processors, recent vector processors, vectorization and optimization methods

UNIT – III (12+4)
Multiprocessors and Multicomputers: Multiprocessor System Interconnects, Cache Coherence and Synchronization Mechanisms, Three Generations of Multicomputers, Message Passing Mechanisms


UNIT – IV (12+4)
Parallel Models, Languages, and Compilers: Parallel Programming Models, Parallel Languages and Compilers, Dependence Analysis of Data Arrays, Loop Parallelization and Pipelining.

UNIX, Mach, and OSF/1 for Parallel Computers: Multi processor UNIX Design Goals, Master-Slave and Multi threaded UNIX, Multi-Computer UNIX Extensions, Mach/OS Kernel Architecture.

Text Books:

Reference Books:

Course Learning Outcomes:
After completion of the course the student will be able to
- Understand multiprocessor Architectures
- Understand pipelining parallelism and vector processors
- Understand multi computer communication
- Understand multithread architectures
P14VE206C  Internet of Things

Class: M.Tech. II Semester  Branch: VLSI & Embedded Systems

Teaching Scheme:  Examination Scheme:

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Continuous Internal Evaluation: 40 marks
End Semester Exam : 60 marks

Course Learning Objectives:
- To introduce challenges and opportunities of Internet of things and applications using wireless sensor networks
- To introduce different protocols for wireless networks
- To expose the basics of integrating internet services
- To introduce good examples of user interaction design

UNIT – I (12+4)

UNIT – II (12+4)

UNIT – III (12+4)
Integrating Internet Services - XML and JSON. HTTP APIs for accessing popular Internet services (Facebook, Twitter, and others). Review the basics of IPv6, Neighbor Discovery, and Stateless Address Auto configuration. Basic operations of 6LoWPAN,

UNIT – IV (12+4)
User Experience And Interaction Design- The three levels of user engagement: aesthetics, functional and emotional. Good examples of user interaction design. Designing your own user experience. Review the whole protocol stack for the classical Internet and the Internet of Things,
Text Books:


Course Learning Outcomes:
After completion of the course the student will be able to

- Learn challenges and opportunities of internet of things
- Understand basic prototyping connected objects.
- Understand integrated internet services
- Understand examples of interaction design
P14VE206D Introduction to MEMS

Class: M.Tech. II Semester  Branch: VLSI & Embedded Systems

Teaching Scheme:

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Examination Scheme:

- Continuous Internal Evaluation: 40 marks
- End Semester Exam: 60 marks

Course Learning Objectives:

- To introduce the basic concepts of micro fabrication and micromachining
- To learn about the Physical Microsensors and Microactuators.
- To analyse the Success Stories of micromachining and micro sensors such as printer heads, Micro-mirror TV Projector.
- To learn the concepts of Micromotors, Gear trains, Mechanisms and applications

UNIT - I (12+4)
Historical Background: Silicon Pressure sensors, Micromachining, MicroElectro Mechanical Systems.; Microfabrication and Micromachining : Integrated Circuit Processes, Bulk Micromachining : Isotropic Etching and Anisotropic Etching, Wafer Bonding, High Aspect-Ratio Processes (LIGA);

UNIT – II (12+4)
Physical Microsensors : Classification of physical sensors, Integrated, Intelligent, or Smart sensors, Sensor Principles and Examples : Thermal sensors, Electrical Sensors, Mechanical Sensors, Chemical and Biosensors.;Microactuators : Electromagnetic and Thermal microactuation, Mechanical design of microactuators, Microactuator examples, microvalves, micropumps, micromotors - Microactuator systems:

UNIT – III (12+4)
Success Stories, Ink-Jet printer heads, Micro-mirror TV Projector; Surface Micromachining: One or two sacrificial layer processes, Surface micromachining requirements, Polysilicon surface micromachining, Other compatible materials, Silicon Dioxide, Silicon Nitride, Piezoelectric materials, Surface Micromachined Systems:

UNIT - IV (12+4)
Micromotors, Gear trains, Mechanisms; Application Areas: All-mechanical miniature devices, 3-D electromagnetic actuators and sensors, RF/Electronics devices, Optical/Photonic devices, Medical devices e.g. DNA-chip, micro-arrays.; Lab/Design:(two groups will work on one of the following design project as a part of the course).;RF/Electronics device/system, Optical/Photonic device/system, Medical device e.g. DNA-chip, micro-arrays.
Text Books:

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<tr>
<td>After completion of the course students will be able to</td>
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<tr>
<td>- To understand the basic concepts of micro fabrication and micromachining</td>
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<td>- To be able to learn about the Physical Microsensors and Microactuators.</td>
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<tr>
<td>- To understand the success stories of micromachining and microsensors such as printer heads, Micro-mirror TV Projector.</td>
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<tr>
<td>- To learn the concepts of Micromotors, Gear trains, Mechanisms and applications</td>
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P14VE207 Embedded System Design Laboratory

Class: M.Tech. II Semester Branch: VLSI & Embedded Systems

Teaching Scheme:

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Examination Scheme:

| Continuous Internal Evaluation: | 40 marks |
| End Semester Exam: | 60 marks |

Course Learning Objectives:
- To introduce the concepts of System C
- To realize the programs by using System C
- To introduce the UML Modeling techniques.
- To implement inter-process communication techniques

List of Experiments:
1. Design All Basic Logic Gates Using SystemC
2. Design Finite State Machines and Sequence Detector Using SystemC
3. Simple Bus Model using SystemC
4. System level Modeling and Design using UML 2.0 Profile
   - i. Composite Structure Diagrams
   - ii. Interaction Overview Diagrams
   - iii. Sequence Diagrams
   - iv. State hart Diagrams
   - v. Timing Diagrams
   - vi. Class Diagrams
   - vii. Code Generation from Class
   - viii. Diagrams and State hart Diagrams
5. Implementing IPC Mechanisms using SystemC
6. Serial Communication Programming
7. Writing Device Drivers
8. RTOS Programming
9. Mini Project-2

Note: As a part of this Laboratory course students has to takeup TWO mini projects.

Report is to be submitted

Course Learning Outcomes:
After completion of the course students will be able to
- Realize programs using concepts of System C
- design the different gates by using System C.
- draw the UML diagrams.
- Implement inter-process communication techniques.
P14VE208  Mixed Signal Design Laboratory

Class: M.Tech. II Semester
Branch: VLSI & Embedded Systems

Teaching Scheme:  
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Examination Scheme:

- Continuous Internal Evaluation: 40 marks
- End Semester Exam: 60 marks

Course Learning Objectives:
- To introduce all basic building blocks like sources, sinks, mirrors.
- To introduce different types of amplifiers and comparators.
- To simulate the characteristics of CMOS inverters

List of Experiments:
1. Common Source Amplifier
2. Simple MOS Current Mirror
3. Cascode Current Mirror
4. Wilson and Widlar Current Mirrors
5. Differential Amplifier (Single Stage)
6. Comparator & CMOS inverters
7. Folded Cascade OP-AMP
8. Bandgap Preference – Current Reference
9. Mini Project – 2

Note: As a part of this Laboratory course students has to takeup TWO mini projects.

Report is to be submitted

Course Learning Outcomes:
After completion of the course students will be able to
- design all basic building blocks like sources, sinks, mirrors up to layout level.
- Simulation of transfer characteristics of MOSFETs using EDA Tools.
- Simulation of transfer characteristics BJTs using EDA Tools
P14VE209 Comprehensive Viva-Voce

Class: M.Tech. II Semester  
Branch: VLSI & Embedded Systems

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<td>Continuous Internal Evaluation:</td>
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<td>End Semester Exam :</td>
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There shall be only external oral examination for Comprehensive Viva-voce on a pre-notified date.

The oral examination shall cover the entire content of courses covered in First and Second Semesters.
P14VE301  Industrial Training

Class: M.Tech. III Semester  Specialization: VLSI & Embedded Systems

Teaching Scheme:

<table>
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Examination Scheme:

| Continuous Internal Evaluation: | 100 |
| End Semester Exam:              | ---  |

1 M.Tech. Coordinator in consultation with the Training & Placement Section will procure training slots, for the students before the last day of instruction of 2nd semester.

2 The students shall confirm their training slots by the last day of 2nd semester.

3 The students after 8 weeks Industrial Training shall submit a certificate, a report in the prescribed format before the last date specified by the Department Post Graduate Review Committee (DPGRC).

4 A oral presentation is to be given before DPGRC.

The DPGRC shall evaluate their submitted reports and oral presentations.
P14VE302  Dissertation

Class: M.Tech. III Semester  Specialization: VLSI & Embedded Systems

Teaching Scheme:  Examination Scheme:

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Continuous Internal Evaluation: 100 marks  End Semester Exam: -

Dissertation in III semester contains two presentations

1  **Registration Seminar** shall be arranged within four weeks after completion of the Industrial Training and Seminar in the 3rd semester. The Registration Seminar shall include a brief report and presentation focusing the identified topic, literature review, time schedule indicating the main tasks, and expected outcome.

2  **Progress Seminar-I**: At the end of first stage (third semester), student shall be required to submit a preliminary report of work done for evaluation to the project coordinator and present the same before the DPGRC.
P14VE401 Dissertation

Class: M.Tech. IV Semester
Teaching Scheme:

<table>
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Specialization: VLSI & Embedded Systems
Examination Scheme:

<table>
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<tr>
<th>Continuous Internal Evaluation:</th>
<th>40</th>
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<tbody>
<tr>
<td>End Semester Exam:</td>
<td>60</td>
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The students are required to present the dissertation work at various stages as follows:

1. Progress Seminar-II shall be arranged during the 6th week of IV semester.
2. Progress Seminar-III shall be arranged during the 15th week of IV semester.
3. Synopsis Seminar shall be arranged two weeks before the final thesis submission date. The student shall submit a synopsis report covering all the details of the works carried out duly signed by the Dissertation Supervisor.
4. At the end of second stage (fourth semester), student shall be required to submit two bound copies, one being for the department and other for the Dissertation Supervisor. The Dissertation report shall be evaluated by the DPGRC.
5. An external examination shall be conducted on a pre-notified date.